

11-26-04

23 November 2004

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JRW

COMMISSIONER FOR PATENTS
Box 1450
Alexandria, Virginia 22313-1450

Application No.: 10/054,653 Confirmation No.: 9448
First Named Inventor: Bulucea, Constantin Filing Date: 18 January 2002
Group Art Unit: 2814 Examiner: Farahani, D.
Atty. Docket No.: NS-5127 US
Title: Gate-Enhanced Junction Varactor With Gradual Capacitance Variation
Assignee(s): National Semiconductor Corporation

Sir:

Transmitted herewith are the following documents for the above patent application:

1. Return Receipt Postcard;
2. This Transmittal Letter (in duplicate);
3. Supplemental Amendment (17 pp.).

The fee has been calculated as shown below:

CLAIMS AS AMENDED

Claims Remaining <u>After Amendment</u>		Highest No.						
		Previously Paid For		Present Extra		Rate		Additional Fee
Total Claims	86	Minus	68	=	18	x	\$18.00	\$ 324.00
Independent Claims	5	Minus	6	=	0	x	\$86.00	\$ 0.00
<input type="checkbox"/> Fee of \$280 for the first filing of one or more multiple dependent claims							\$	
<input type="checkbox"/> Fee for Request for Extension of Time (month(s))							\$	
<input type="checkbox"/> Fee for							\$	
<u>Total additional fee for this Amendment:</u>							\$	324.00
<input checked="" type="checkbox"/> Please charge Deposit Account No. 502641 in the amount of							\$	324.00
<input checked="" type="checkbox"/> Conditional Petition for Extension of Time: If an extension of time is required, the Commissioner is authorized to deduct the necessary fee from Deposit Account No. 502641.								
<input checked="" type="checkbox"/> Also, charge any additional fees required and credit any overpayment to Deposit Account No. 502641.								

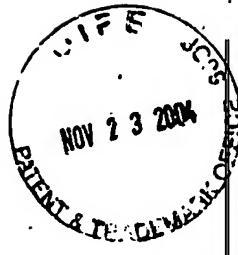
EXPRESS MAIL LABEL NO.:

EV 500 310 505 US

Respectfully submitted,

Ronald J. Meetin
Attorney for Applicant(s)
Reg. No. 29,089

210 Central Avenue
Mountain View, California
Tel.: 650-964-9767



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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SUPPLEMENTAL AMENDMENT

Sir:

Further to the Amendment submitted 11 June 2004 in response to the Office Action mailed 12 February 2004, please amend the above patent application in the following manner.

IN THE CLAIMS

Add new Claims 75 - 94 so that the claims are as follows:

1. (Previously amended) A structure comprising:
a varactor comprising (a) a plate region and a body region of a semiconductor body,
(b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of

Ronald J. Meitin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

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